Amendments to the Specification:

On pages 5 - 6 of the specification, please amend the paragraph beginning on line 33 of page 5 as follows:

A method of determining a [[a]] start of a transmitted frame at a receiver on a frame-based communications network is provided. A preamble format for the transmitted frame is provided wherein a plurality of identical copies of a preamble symbol sequence are transmitted sequentially. A received transmitted frame is filtered using filter coefficients matched to the preamble symbol sequence to provide a correlation sequence. A squared-magnitude of the correlation sequence is computed. The squared-magnitude of the correlation sequence is low-pass filtered to provide a low-pass filtered correlation ~~signallow-pass filtered~~ signal. The low-pass filtered correlation signal is delayed to provide a delayed low-pass filtered correlation~~ signal.The~~ signal. The delayed low-pass filtered correlation signal is multiplied by a first fixed predetermined threshold to provide a multiplied correlation signal. The multiplied correlation signal is compared with the low-pass filtered correlation signal to provide a correlation difference indicator. Energy of the received transmitted frame is detected and the energy is low-pass filtered to provide a low-pass filtered energy signal comparing detected energy to a fixed energy threshold to provide a threshold compared energy signal. The low-pass filtered energy signal is multiplied by a second fixed predetermined threshold to provide a multiplied energy signal. The threshold compared low-pass filtered correlation signal is compared with the threshold compared ~~mulitiplied~~ multiplied energy signal to provide a correlation peak indicator. A logical-AND of the correlation difference

indicator and the correlation peak indicator is formed to determine a match/no match comparison indicative of the start of a transmitted frame.

On pages 85 - 87 of the specification, please amend the paragraph beginning in line 26 of page 85 as follows:

Now turning to the carrier sense function in more detail, a preferred carrier sensing embodiment which is particularly useful for severely-distorted networks is described. On a typical Ethernet bus, all taps are terminated in the characteristic impedance of the line to minimize reflected signal power. Because reflections are insignificant and the signal-to-noise ratio (SNR) at each receiver is very high, a simple carrier sense technique (e.g. level detector with a fixed threshold) may be used to determine when the medium is busy. In residential networking over pre-installed wiring (e.g. phone wiring, power wiring), attenuation may be high due to wall jacks and unused wire segments that are not terminated with the characteristic impedance of the wire. There will also be severe reflections for the same reason. The receiver SNRs may be low (10 dB or lower in some cases). In addition, the problem is complicated by the fact that every path between two stations on the network has a different channel impulse response. On one path, two stations may communicate at a high rate (e.g. 8 bits/symbol), while all other paths only support 2 bits/symbol. The implication of this example is that the demodulator may not be used as the method of carrier sense in such a network, as all stations on the network are able to delineate frames, even those whose payloads may not be demodulated due to insufficient SNR. Beyond even these complications, there is impulse noise, which may result in false carrier detection with certain types of detectors. In accordance with the present invention a detector

is provided for precisely determining the start of a frame (within 1 microsecond) in a severely-impaired CSMA/CD network. In addition, this detector determines the start of a frame with sufficient precision to generate a channel model with a small number of adjustable coefficients for generating decision-feedback equalizer weights. In ~~accordnace~~ accordance with the present invention, a preamble format is provided in which M identical copies of the same k*n-symbol quadrature phase-shift keying (QPSK) sequence are transmitted sequentially. This k*n-symbol sequence is spectrally white over an k*n-symbol span (has a single non-zero circular autocorrelation value). Further, the k*n-symbol QPSK sequence consists of k sequentially-transmitted copies of an n-symbol subsequence that is spectrally white over an n-symbol span. Further, a detector for precisely determining the end of a frame (within a 4- microsecond window) in a severely-impaired CSMA/CD network is provided. In accordance with the present invention an n-symbol sequence that is spectrally white over an n-symbol span that delimits the end of a burst and enables this detector is provided. By keeping the end-of-frame detection uncertainty low, the efficiency of the network is increased.

On page 89 of the specification, please amend the paragraph beginning in line 4 as follows:

With regard to the low-delay detector in Fig. 57, it uses a filter matched to the first n symbols of the preamble. The filter coefficients are the first n symbols of the preamble in reverse order, complex-conjugated, then interspersed with L zeros per symbol. If the first n symbols are $[s_0, s_1, \ldots s_{(n-1)}]$, then the filter coefficients are $[s_{(n-1)}^*, 0, 0, 0, s_{(n-2)}^*, 0, 0, 0, \ldots s_0^*, 0, 0, 0]$, when L = 4. "*" indicates complex conjugation of the symbol value. The bit widths, shown in Fig.

57 as r, r+1, q, etc., are merely examples in one particular embodiment, and the invention is not limited to any particular datapath widths. "j" is the sample (time) index in Fig. 57. Note that, because the preamble consists of only QPSK symbols, no multiplications (only additions and subtractions) are required. The output of the MA block is computed as $\max(x_i, x_q) + \frac{1}{2} * \min(x_i, x_q)$, where x_i is the in-phase component of the complex sample and x_q is the quadrature component, with rounding. The output of the matched filter in this one embodiment saturates at r+1 bits twos-complement, but other outputs are possible within the scope of this invention. AVG may be either a simple L*n-sample moving average or a one-pole smoothing filter with alpha = 1/(L*n).

On pages 91 - 92 of the specification, please amend the paragraph beginning in line 7 of page 91 as follows:

Referring back to Fig. 59, specific operational aspects of the start of frame detection are described in more detail. One aspect is the start of frame detection. In upper portion 3010 the first stages of carrier sense / start of preamble detection is shown. In lower portion 3012 the remaining stages are shown. Accordingly, the carrier sense processing starts at the upper left portion of Fig. 59 and ends at the lower right portion of Fig. 59. Input 3014 has r bits, which in a preferred embodiment is at 8Msamples/sec. Matching filter/correlator 3016 receives the r bits, and filters the input using filter coefficients which are a time-reversed sequence copy of the preamble sequence. The output of filter 3016 is provided to magnitude approximator 3018 and squaring function 3020. Magnitude approximator 3018 provides a real output for which on one squaring operation is ~~needeed~~ needed, avoiding the need for a multiplier function. The output of squaring function 3020 is

input to low-pass filter 3022. Low pass filter 3022 smoothes the input thereto and provides output Z_j. At input 3014 r is also fed into an energy detection computation where magnitude approximation 3024 is performed, then a squaring operation 3026, then a longer duration low-pass filtering 3028, and then performing a low-pass filtering operation 3030 comparable to that of low-pass filter 3022, providing an output zh_j. Z_j is then put through logarithm function 3032 to allow measuring of ratios avoiding division operations. zh_j[[Z_{hj}]] is similarly put through logarithm function 3034. ~~The output from logarithm function 3032.~~ Two tests are performed during the carrier sense computation at compare functions 3036 and 3038. Where inputs A and B respectively are compared based upon a threshold, e.g., 9dB threshold input into compare function 3036 and 3dB threshold input into compare function 3038. In other words a calculation is performed to determine if A - B is > than the threshold. Delays [[3040]]3033, [[3042]]3035, [[3044]]3037 are provided between the logarithm functions and the compare functions. In essence, with regard to the Z_j processing of portion 3012, the smoothed low-pass filtered output of the matched filter is compared with a delayed copy of itself, as provided by delay [[3040]]3033. In addition delay function [[3044]]3037 is applied to the output of logarithm function 3032 providing a slightly delayed input to compare function 3038. With regard to the [[zhj]]zh_j processing, delay function [[3042]]3035 and maximizing function [[3046]]3039 is applied to the output of logarithm function 3034 to provide a sampled maximum to avoid getting a false trigger. Therefore compare function 3038 compares whether [[that]]the smoothed low-pass filtered output is greater than the [[Z_{hj}]]zh_j output of the energy detector. The output of comparator functions 3036 and 3038 is then provided to AND

function 3040, a match if both inputs are true and a no match if one is not true.

On pages 170 - 171 of the specification, please amend the paragraph beginning in line 27 of page 170 as follows:

Fig. 80, which, depicts components of an embodiment an HPNA TRC circuit in accordance with the present invention, is now described in more detail. Adder [[3010]]4010, reference clock signal [[3012]]4012 and NCO [[3014]]4014 are provided. An output from the NCO [[3014]]4014 is fed into integer divider [[3016]]4016. This clock in the slave device gets divided down to 8kHz (V_CLK_OUT) [[3018]]4018 since it is running at much higher speed to maintain an accuracy. The V_CLK_OUT feeds the sampling circuitry of the CODEC. The software makes a determination as to whether the clock is running fast or slow via SNOOP_BUS [[3020]]4020 which is located inside the transceiver which allows the software to communicate with the hardware. The PCI bus writes a value to register [[3022]]4022. Synchronizer [[3024]]4024 is provided to make sure that the change in register [[3022]]4022 is synchronous to the NCO [[3014]]4014. The output clock gets speeded up or slowed down depending on the value loaded into register [[3022]]4022. The software looks at the timestamps that are received at the slave and determines if the slave clock is running slow or fast. It makes an adjustment to the register [[3022]]4022 value which adjusts the speed of the NCO [[3014]]4014. It does this typically every one second, or whatever time is necessary for a defined accuracy.

On pages 172 - 173 of the specification, please amend the paragraph beginning in line 7 of page 172 as follows:

The grant timing that is determined from the DOCSIS network is delivered directly to the transceiver for the HPNA. That information is gathered by the timestamp circuit on the master and input to the circuit via Grant(4)timing signal, with S_GRANT enabling the path. Grant [3:0] allows multiple different grant identifiers (one of sixteen) to be selected. When the interested in grant identifier sees it's grant, that latches the timestamp. Therefore, when a grant occurs there is a timestamp associated with the grant at the master. The master then reads that timestamp information, puts it into a packet and delivers that packet with the grant timestamp identifiers associated with it to all the nodes. The node associated with that particular grant identifier picks up the information and now it knows when its grant occurred. It will have been able to relate its time to the master's time by looking at the offset between the time it received according to its clock and the master's time. For example, using human time differentials, if the master indicates that it sent a packet at 12:00 o'clock, and the slave indicates that it received the packet at 3:30 o'clock, it knows that the two clocks differ by 3 ½ hours. Since it knows that it is 3 ½ hours off, then when the master latches a grant time in its timestamp register, when it delivers that time the slave then knows that it needs to adjust the time by 3 ½ hours to make it updated to its local time. Once it knows the local time of the grant, then it adjusts that backwards by the time it needs to assemble the packet and deliver it on the HPNA network. It works backwards to figure out what the latest time is that it should send that packet out of the network. It puts that time into a GRANT_TIME register [[3030]]4030 and when the local time in the slave matches at a exclusive-OR comparator [[3032]]4032 an output signal Frame[0] is created which goes to the voice CODEC and tells it to deliver 80 samples. In fact, the signal Frame[0]

can be sent to any portion of the circuit which is making the actual decision as to when to call a set of 80 samples a frame. The circuit also automatically updates the grant time period rate, e.g., 10 msec, such that when the grant time matches the current local time, 10 msec is automatically added to the grant time and 10 msec later another match of the grant time with the current local time and the framing signal will be created again.

On pages 173 - 174 of the specification, please amend the paragraph beginning in line 13 of page 173 as follows:

Of note is that the NCO error input is calculated by the device driver. The BIAS is added to the error, and the driver writes the resulting value to the NCO_INC register [[3022]]4022. The correct BIAS value depends upon the V_CLK_OUT frequency requirement for the specific application. The V_CLK_OUT signal must be square (50% duty cycle). The V_CLK_OUT signal will begin with a default rate at power up. During RESET, the rate will be fixed. After RESET, the software will write values to various control bits that may change the rate of the V_CLK_OUT signal. These changes must not produce glitches on the V_CLK_OUT output. The circuit as depicted allows V_CLK_OUT frequencies in the range: mear DC to 100MHz. However, because of the requirement for the timestamp to be running at 4.096 MHz, an additional requirement must be placed on the V_CLK_OUT signal. The V_CLK_OUT signal must either be a ratio of integers divide of 4.096MHz, or it must be a ratio of integers multiple of 4.096MHz, where the integers must be in the range of 1-255, inclusive. This should provide sufficient range of V_CLK_OUT operation for all expected applications. The accuracy of the DPLL decreases as the output frequency is reduced because the rounding error remains constant in magnitude, while the control word value decreases in magnitude. For a direct conversion of

200MHz to 8kHz, the control word for a 32-bit DPLL is 29F16, which produces a rounding error of 4ppm. If this rounding error is unacceptable, then any of several remediation steps can be taken, including, adding bits to the DPLL register. Adding 2 bits to the register changes the error to 1.1ppm. Another option is to perform less conversion in the DPLL, then feed the DPLL output to a divider to get the final output. It turns out that additional divide steps are required anyway, because a fixed rate clock is required for the timestamp function. The fixed rate for the timestamp is chosen to be 32.768MHz. (If the timestamps at the master and slave differ by a power of two, this would be acceptable, since software could accommodate the difference. Some other integer relationships are easy to adapt in a simple CPU -- for example, the factor of 6 is easily obtained by two additions.) The chart set forth in Fig. 81 shows the jitter in the DPLL output when the reference clock is 200MHz and the DPLL output clock (CNT[31]) is 32.768MHz. The jitter variance is +/-2.5ns and the frequency of the jitter is about 3.3MHz. The jitter frequency is well above the audio range, and the +/-2.5ns causes noise that is below -70dB in amplitude, thereby allowing the A/D to achieve the required 35dB SNR requirement of ITU-T recommendation G.712. Lower frequency components do exist in the jitter waveform, but the amplitude of these components is significantly lower than the 3.3MHz signal. The offset of the jitter shown in Fig. 81 is corrected over time by DPLL frequency adjustments, such that the offset will ultimately vary around 0.

On pages 174 - 175 of the specification, please amend the paragraph beginning in line 28 of page 174 as follows:

Referring back again to Fig. 80, to determine the master timestamp, DPLL_REF_CLK [[3040]]<u>4040</u> is a fixed clock provided

for register [[3014]]4014. It is considered the "master clock" to which other devices are to be synchronized. After dividers [[3016]]4016 and [[3019]]4019 divide the signal from register [[3012]]4012 to provide TS_CLK [[3042]]4042 which drives timestamp register [[3011]]4011, which is the source of the timestamp for the packet. The output of timestamp register [[3011]]4011 is provided to TX_TSTAMP register [[3044]]4044 which takes the timestamp in response to its EN becoming active. EN becomes active when TX_SIG [[3046]]4046 is asserted at a fixed point in the transmission, e.g., at the end of preamble. The output of TX_TSTAMP register [[3044]]4044 is made available to software through register access on the device.

On page 175 of the specification, please amend the paragraph beginning in line 8 as follows:

Still referring to Fig. 80, on the slave side receives a packet. The timestamp at reception has no known relationship to the master timestamp other than counting at the same rate. Analogous to the timestamp operation described above, when RX_SIG [[3048]]4048 is asserted at a fixed point in the transmission, e.g., at the end of preamble, which agrees with the master side fixed point, which enables the load operation of RX_TSTAMP [[3013]]4013 of whatever is then in its TIMESTAMP register [[3011]]4011. The output of RX_TSTAMP register [[3013]]4013 is similarly made available to software.

On pages 175 of the specification, please amend the paragraph beginning in line 17 as follows:

Referring back to the master aspect of Fig. 80, the transmitter software reads the latched output of TX_TSTAMP [[3044]]4044 and puts the value into a subsequent packet and

sends the packet along to the slave device. The slave device receives the sent packet it reads its latched output from RX_TSTAMP [[3013]]4013 and determines when the event occurred on the receive side.

On pages 176 - 177 of the specification, please amend the paragraph beginning in line 22 of page 176 as follows:

Referring again to Fig. 80, NCO incrementer [[3022]]4022, in response to error input from software, filtered an biased by software, adjusts the feed of the count of NCO [[3014]]4014. This helps compensate for drifting frequency between slave and master. With NCO incrementer [[3022]]4022 set to the nominal reset value, NCO [[3014]]4014 halves the frequency of the DPLL reference clock. TS_SCALE register [[3070]]4070 and V_SCALE register [[3072]]4072 along with integer dividers [[3016]]4016, [[3019]]4019 are used to allow at the slave side different crystal frequencies that don't match the crystal frequencies at the master side. The outputs from NCO [[3014]]4014 and dividers [[3016]]4016 and [[3019]]4019 provides clock [[3018]]4018 which feeds the CODEC clock which takes samples of the analog stream, the dividers helping create a slower clock for the CODEC. Further, signal Frame [0] signal [[3074]]4074 is also provided to the CODEC to indicate to the CODEC when to slice off a set of samples for packetization, based upon the transmit opportunity times as to when a set of samples is to be assembled into a packet. GRANT_PRD register [[3017]]4017 is loaded with signals representative of the periods of the transmit opportunities. When GRANT_TIME register [[3030]]4030 initial grant time loaded becomes the same as TIMESTAMP register [[3011]]4011, a true compare output is provided to enable a reload of GRANT_TIME register [[3030]]4030 to reload grant time plus grant period output from 32 bit adder [[3076]]4076. With the computation of

the grant period offset, the next transmit opportunity time in the future for a transmission to occur is provided, and signals the CODEC that a time has arrived to assemble a packet for queuing for transmission.

On pages 177 of the specification, please amend the paragraph beginning in line 16 as follows:

Still referring to Fig. 80, with regard to the master side operation S_GRANT signal [[3078]]4078 is an enabling signal and Grant [4] [[3080]]4080 is received from the DOCSIS side of the network, a synchronous timing event. When this occurs the current timestamp is latched into TX_TSTAMP register [[3044]]4044.